In the Written Description:

Page, 1, beginning at line 1, Amend the "Title of the invention" as follows:

METHOD FOR DESIGNING SEMICONDUCTOR CIRCUIT DEVICE, UTILIZING BOUNDARY CELLS BETWEEN FIRST AND SECOND CIRCUITS DRIVEN BY DIFFERENT POWER SUPPLY SYSTEMS~~SEMICONDUCTOR CIRCUIT DEVICE, DESIGN SYSTEM, AND STORAGE MEDIUM~~

On page 6, paragraph beginning at line 11, amend as follow:

According to a second aspect of the present invention, there is provided a semiconductor circuit device designed by the above described design a method ~~of designing a semiconductor circuit device according to Claim 1~~.

On page 6, paragraph beginning at line 25, delete entire paragraph as follows:

~~According to a fourth aspect of the present invention, there is provided a semiconductor circuit device designed by a method of designing a semiconductor circuit device according to Claim 10.~~

On page 2, paragraph beginning at line 21, amend as follows:

In this circuit structure, while the second power supply for the output circuit is OFF, the output of the control unit in the input circuit is kept Low, thereby preventing the shoot-through current from occurring in the input circuit. If the second power supply turns from ON to OFF when the output signal from the CMOS inverter is High, the output signal of the CMOS inverter turns from High to Low through an intermediate level. Since the output of the control unit turns to Low when the second supply voltage falls below the given voltage, no shoot~~short~~-through current occurs in the input circuit. The power consumption is thereby reduced.

On page 4, paragraph beginning at line 19, amend as follows:

In the first aspect of the present invention, the boundary circuit preferably includes a circuit for suppressing shoot~~short~~-through current between the first circuit and the second circuit when one of the first circuit and the second circuit is off and the other one of the first circuit and the second circuit is on. This enables effective design of a circuit for suppressing shoot~~short~~-through current between circuits driven by different power supplies. Alternatively, the boundary circuit preferably includes a circuit for preventing circuit malfunction due to indeterminate current between the first circuit and the second circuit when one of the first circuit and the second circuit is off and the other one of the first circuit and the second circuit is on. This enables effective design of a circuit for preventing circuit malfunction due to indeterminate current between circuits driven by different power supplies.

On page 12, paragraph beginning at line 14, amend as follows:

Referring now to Figs. 2A and 2B, a shoot-through current suppression circuit 200 is shown as an example of the boundary circuit. Fig. 2A is a logic circuit diagram showing the circuit configuration of the shoot-through current suppression circuit 200. Fig. 2B shows a truth table for the shoot-through current suppression circuit 200. Use of the shoot-through current suppression circuit 200 can suppress the transmission of an indeterminate signal from a circuit area where power supply is OFF to a circuit area where power supply is ON. The use of this circuit can substantially prevent the indeterminate signal. This allows suppressing or preventing a shoot~~short~~-through current to occur in the next-stage circuit to reduce the power consumption of the entire chip.

On page 13, paragraph beginning at line 7, amend as follows:

The operation of the shoot~~short~~-through current suppression circuit 200 will be explained with reference to Figs. 2A and 2B. Fig. 2B shows the relationship of an input signal "input" to the input terminal 201, an enable signal "enable" to the enable terminal 204, and an output signal "output" from the output terminal 205. The symbol "X" in the table indicates that a signal is indeterminate, "0" indicates that the output voltage is Low, and "1" indicates that the output voltage is High. If the first circuit area 101 is OFF, an indeterminate signal is input to the input terminal 201.

On page 13, paragraph beginning at line 17, amend as follows:

Specifically, if the first circuit area 101 is OFF, the output signal from the first circuit area 101 to the second circuit area 102 is indeterminate between High and Low. Thus, a signal with an intermediate voltage level is input to the second circuit area 102. This causes the shoot~~short~~-through current to occur in the second circuit area 102. To prevent this, this

embodiment controls the operation in such a way that the enable signal input to the NAND gate 203 is "0", which is "Low", when the first circuit area 101 is OFF.

On page 14, paragraph beginning at line 2, amend as follows:

By setting the enable signal to "0", it is able to determine and keep the output signal from the output terminal 205 to be "1", that is, the output voltage to be "High". As described above, if the circuit is OFF, its output is indeterminate between High and Low, and thus a signal with an intermediate voltage level between High and Low is input to the receiving circuit. The circuit configuration in this embodiment, however, can suppress the shoot~~short~~-through current in the ON-state circuit area due to the indeterminate signal from the OFF-state circuit area.

On page 12, paragraph beginning at line 12, amend as follows:

If the first circuit area is ON, the shoot~~short~~-through current suppression circuit 200 is controlled in such a way that the enable signal is "1". Thereby, if the input signal from the internal circuit of the first circuit area 101 to the input terminal 201 is "0", the output signal from the output terminal 205 to the internal circuit of the second circuit area 102 is determined to be "0", and if the input signal is "1", the output signal is "1". If the input signal is indeterminate and the enable signal is "1" or indeterminate, the output signal is indeterminate.

On page 18, paragraph beginning at line 21, amend as follows:

Though several examples of the boundary circuit are shown above, the boundary circuit to which the present invention is applicable is not limited thereto. The above circuits may be inserted between the circuit areas driven by different power systems separately or in combination with others. For example, it is possible to insert the level conversion circuit or

the ESD protection circuit without using the shoot~~short~~-through current suppression circuit. It is also possible to insert the boundary circuit including both the level conversion circuit and the ESD protection circuit. In each boundary circuit, the circuit driven by the first power supply may be viewed as included in the first circuit area, and the circuit driven by the second power supply may be viewed as included in the second circuit area.

On page 21, paragraph beginning at line 11, amend as follows:

Then, the design tool 601 inserts the boundary cell into the gate-level netlist 722, referring to the gate level boundary cell library 752. The design tool 601 specifies the circuit areas with different power supplies in the gate-level netlist 722 and inserts an appropriate boundary cell as designed on a signal transmission path between the circuit areas. The boundary cell to be inserted may be the shoot~~short~~-through current suppression circuit cell, the leakage current suppression circuit cell, or a level shifter, for example. A gate-level netlist 723 including the boundary cell is thereby created. The netlist contains boundary circuit information and boundary circuit connection information in addition to information on a plurality of circuit areas driven by different power systems. The gate-level cell libraries 751 and 752 contain information on cell functions, delays, and input/output pins, for example.